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-	6	two adj1 stage\$1 adj1 equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 08:29
-	7	((two or more or multi\$3) with stage\$1) with equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 11:55
-	6	((two or more or multiple) adj1 stage\$1) with equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 11:49
-	7	((two or more or multi\$3) adj1 stage\$1) with equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 11:50
-	20	((two or more or multi\$3) adj1 stage\$1) with equalizer and trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 11:50
-	1	.	USPAT	2004/09/22 11:55
-	3	(forward and decision adj1 feedback) with equalizer same trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 16:07
-	155	(forward and decision adj1 feedback) with equalizer and trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:36
-	7	(first and second) with (forward and decision adj1 feedback) with equalizer and trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:58
-	19	"5692011"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:15
-	25	"5539774"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:30
-	6	"6418164"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:31
-	6	"6411659"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:33
-	13	"6307901"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:35
-	16	"6253345"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:37
-	7	"6246723"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:38
-	8	"6201832"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:39
-	6	"6035428"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:41

-	22	"5572262"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:44
-	28	"5513215"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:48
-	13	"5453797"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:50
-	35	"5414738"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:51
-	1	((first and second) or dual) with forward adj1 equalizer and decision adj1 feedback adj1 equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 14:59
-	11	forward adj1 equalizer and decision adj1 feedback adj1 equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:05
-	38	((forward adj1 equalizer) or \$1FE) and ((decision adj1 feedback adj1 equalizer) or DFE) with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:07
-	6	((two or dual or multiple or multi) adj1 stage\$1) adj1 equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:16
-	6	((two or dual) adj1 stage\$1) adj1 equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:16
-	7	((two or dual or multiple or multi) adj1 stage\$1) with equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:22
-	18	(dual or more or multi\$3 or serial) with equalizer with trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:40
-	20	((two or dual or multiple or multi) adj1 stage\$1) with equalizer and trellis adj1 cod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:38
-	204	((two or dual or multiple or multi) adj1 stage\$1) with equalizer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:23
-	3	((two or dual) adj1 stage) or multi\$1 adj1 stage\$1) adj1 decision adj1 feedback adj1 equalizer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:26
-	11	((two or dual) adj1 stage) or multi\$1 stage\$1) adj1 decision adj1 feedback adj1 equalizer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:26
-	19	((two or dual) adj1 stage) or multi\$1 adj1 stage\$1) with (decision adj1 feedback adj1 equalizer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:29
-	8	(forward adj1 equalizer) with decision adj1 feedback adj1 equalizer with trellis adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:44
-	12	((two or dual or multiple or multi) adj1 stage\$1) with equalizer and trellis adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 16:07

-	11	(forward adj1 equalizer) with decision adj1 feedback adj1 equalizer same trellis adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:40
-	65	(dual or more or multi\$3 or serial) with equalizer with trellis adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 07:22
-	11	(forward adj1 equalizer) with (decision adj1 feedback adj1 equalizer) same (trellis adj1 decod\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:46
-	27	(forward adj1 equalizer) with (decision adj1 feedback adj1 equalizer) and (trellis adj1 decod\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:47
-	67	(forward adj1 equalizer) with (decision adj1 feedback adj1 equalizer) and (trellis or viterbi or TCM)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:48
-	14	(forward adj1 equalizer) with (decision adj1 feedback adj1 equalizer) with (trellis or viterbi or TCM)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:47
-	56	(forward adj1 equalizer) with (decision adj1 feedback adj1 equalizer) and (trellis)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 15:48
-	7	((two or dual or multiple or multi) adj1 stage\$1) with equalizer with (trellis or viterbi or TCM) adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 07:49
-	56	(forward and decision adj1 feedback) with equalizer with (trellis or viterbi or TCM) adj1 (cod\$3 or decod\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/22 16:10
-	65	(dual or more or multi\$3 or serial) with (equalizer with trellis adj1 decod\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 07:22
-	21	"5546430"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 08:11
-	12	"6240133"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 08:11
-	10	(birru with dagnachew or philips) and (forward adj1 equalizer with decision adj1 feedback adj1 equalizer) and trellis adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 08:33
-	50	(birru with dagnachew or philips) and equalizer and trellis adj1 decod\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/23 08:33

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[\[Abstract\]](#)   [\[PDF Full-Text \(180 KB\)\]](#)   **IEEE JNL****2 Continuous-time forward equalization for the decision-feedback-equalizer-based read channel***Brown, J.E.C.; Hurst, P.J.;*

Magnetics, IEEE Transactions on , Volume: 34 , Issue: 4 , July 1998

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*Joshi, R.B.; Samueli, H.;*

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**6 A comparison of analog DFE architectures for disk-drive applications**

*Brown, J.E.C.; Hurst, P.J.; Der, L.; Agi, I.;*

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Pages:99 - 102 vol.4

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**7 Performance of electrical equalizers in optically amplified OOK and DPSK systems**

*Jin Wang; Kahn, J.M.;*

Photonics Technology Letters, IEEE , Volume: 16 , Issue: 5 , May 2004

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[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) IEEE JNL

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**8 Adaptive PMD compensation by electrical and optical techniques**

*Buchali, F.; Henning Bulow;*

Lightwave Technology, Journal of , Volume: 22 , Issue: 4 , April 2004

Pages:1116 - 1126

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**9 Mostly analog disk drive read channel with practical depth-of-two fixed delay tree search**

*Wei, D.C.; Sun, D.Q.; Abidi, A.A.;*

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Pages:3689 - 3698

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**10 A CMOS adaptive continuous-time forward equalizer, LPF, and RAM-DFE for magnetic recording**

*Brown, J.E.C.; Hurst, P.J.; Rothenberg, B.C.; Lewis, S.H.;*

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**11 A comparison of two blind equalization algorithms for broadband indoor wireless communications**

*Lin He; Malkemes, R.; Reed, C., Jr.; Amin, M.G.;*

Signal Processing and its Applications, Sixth International, Symposium on. 2001 , Volume: 2 , 13-16 Aug. 2001

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**12 Adaptive equalization for 100 Mbps OWSS wireless LANs**

*Dholakia, J.H.; Jain, V.K.; Myers, B.A.;*

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*Neurohr, N.;*

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**14 Design of multilevel decision feedback equalizers**

*Mathew, G.; Farhang-Boroujeny, B.; Wood, R.W.;*

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*Zukunft, R.; Haar, S.; Magesacher, T.;*

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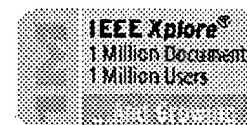
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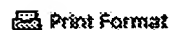
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Pages:933 - 938[\[Abstract\]](#)   [\[PDF Full-Text \(384KB\)\]](#)   **IEEE JNL****2 Recursive bitstream conversion: third-order structures***Roza, E.; Birru, D.;*Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 49 , Issue: 5 , May 2002  
Pages:591 - 601[\[Abstract\]](#)   [\[PDF Full-Text \(495KB\)\]](#)   **IEEE JNL****3 A generalized multirate topology of reduced-sample-rate  $\Sigma\Delta$  modulators with optimum coefficients***Birru, D.;*Signal Processing Letters, IEEE , Volume: 6 , Issue: 8 , Aug. 1999  
Pages:196 - 198[\[Abstract\]](#)   [\[PDF Full-Text \(152KB\)\]](#)   **IEEE JNL****4 A novel delay-locked loop based CMOS clock multiplier***Birru, D.;*Consumer Electronics, IEEE Transactions on , Volume: 44 , Issue: 4 , Nov. 1998  
Pages:1319 - 1322[\[Abstract\]](#)   [\[PDF Full-Text \(432KB\)\]](#)   **IEEE JNL****5 Optimized reduced sample rate sigma-delta modulation***Birru, D.;*Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 44 , Issue: 11 , Nov. 1997  
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